REMARKS

SUPPORT FOR AMENDMENT

Claim 3 has been incorporated into claims 1 and 12. No new matter has been added. Upon entry of this amendment Claims 1, 2, 4-8, 12-16, and 24-26 are present and active in the application.

REQUEST FOR RECONSIDERATION

Chemical mechanical polishing (CMP) is a recognized process for making the upper surface of a dielectric on a semiconductor device planar. In a typical CMP process a wafer is subject to an initial polish for an estimated amount of time such that the thickness does not go below a targeted value. The resulting thickness of the layer is then measured, and using this measured thickness and the initial polishing time, a polish rate is calculated. Finally, the wafer is polished for a time that is calculated to achieve the desired final thickness based on the polish rate.

This process has disadvantages, mainly due to the manual estimates and calculations that are required. Inconsistent thickness targeting can lead to poor process control. It is difficult to account for other parameters which affect the CMP, such as incoming dielectric thickness pattern density, removal rate, and pad hours. Thus, it is difficult to track the overall process to determine the source of errors. The present invention mitigates these problems.

As now claimed, the present invention includes measuring a pattern density of a layer and calculating a polish time sufficient to planarize the layer. This allows for controllably targeting the thickness of a layer by making use of the recognition that the polishing time has two primary components: (i) the time necessary to planarize the layer, and; (ii) the time necessary to reduce the thickness of the planarized layer.

The rejection of the claims under 35 U.S.C. § 102 over Kim et al., or under § 103 over Kim et al. in view of Maekawa, is respectfully traversed. Kim et. al., calculates the effective pattern density of a layer and its thickness prior to and following CMP, and does not teach measuring pattern density.

Kim et al. describes a method and apparatus that calculates the effective pattern density of a planarization layer prior to and following the polishing process. The layout

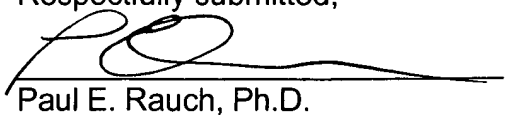
data that defines the patterned layer of an integrated circuit is generated (column 6, lines 25-32). This calculated pattern density is used to further calculate the thickness of the planarization layer prior to and after the CMP (col. 6, lines 33-34; col. 9, line 61, to col. 10, line 2). A CMP simulation is then performed, and integrated circuits may be fabricated using the parameters that are produced from the simulation (col. 6, lines 36-44).

Maekawa teaches that the Cpk value has been monitored in CMP processes, obtaining a process with a Cpk of at least 1.

In contrast, the present invention as now claimed does not calculate, but rather measures the data related to the wafer to be treated (page 6, lines 5 - 15). The measured data include the layer thickness and the pattern density, which may be measured by topographic analysis. The data is used to calculate the polishing time sufficient for planarizing the layer and further reduce its thickness while maintaining its planarity. Thus, Kim et al. is a process based on calculating certain process parameters, whereas the present invention measures the same parameters. Furthermore, Maekawa, either alone or in combination with Kim et al., does not describe calculating a polish time sufficient to planarize a layer, where the calculations are based on measured parameters. Consequently, applicants submit that the claimed invention is neither anticipated by, nor obvious over, the applied references, singly or in combination. Withdrawal of these grounds of rejection is therefore respectfully requested.

Applicants submit the application is now in condition for allowance. Early notice of such action is earnestly solicited.

Respectfully submitted,



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